UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,943	06/24/2003	John Anthony Rodriguez	TI-35492	1788

23494 7590 03/09/2004

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
LEE, HSIEN MING	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 03/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/602,943	RODRIGUEZ ET AL.	
	Examiner	Art Unit	
	Hsien-Ming Lee	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-23 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-23 is/are rejected.

7)☒ Claim(s) 2 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 2 is objected to because of the following informalities: editorial error. In lines 20-21, changing ".... and a ferroelectric material the respective memory cells" into -- and a ferroelectric material **in** the respective memory cells – is suggested.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 6-7, 10-13, 15-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Traynor (US 6,008,659).

In re claims 1, 6, 7, 17, Traynor teaches the claimed method of fabricating a ferroelectric memory device comprising:

- fabricating a ferroelectric memory device having arrays of memory cells via a number of suitable fabrication processes;
- determining a desired data retention lifetime (i.e. determining a short time duration or longer time duration dependent upon the desired capacitor) for the memory cells of the ferroelectric memory device (col. 6, lines 3-7);
- selecting a time parameter and a temperature parameter, as a function of the data retention lifetime, for baking the ferroelectric memory device during a retention test according to the desired data retention lifetime, selecting a particular initial state (i.e.

such as up polarization state, see Fig.5 and col. 58-65) according to the desired data retention lifetime ;

- programming the memory cells of the ferroelectric memory device to be in the selected initial state;
- performing a bake procedure on the ferroelectric memory device with the memory cells programmed to the selected initial state according to the selected time parameter and the selected temperature parameter, i.e. baking the ferroelectric memory device for a cumulative bake time of 20 hours at about 150 °C during the retention lifetime test (col. 6, lines 7-29); and
- performing lifetime testing on the ferroelectric memory device to determine estimated data retention lifetimes for the memory cells (col. 6, line 30 through col. 7, line 31).

In re claims 10-11, Traynor also teaches that the initial state is negative (i.e. down polarization, N pulse) or positive (i.e. up polarization, P pulse) (col. 2, line 65 through col. 3, line 14).

In re claims 12 and 15-16, 18, Traynor further teaches that performing lifetime testing comprises performing a number of lifetime test cycles comprising:

- writing same state data (i.e. Qss) to a first capacitor and a second capacitor of the ferroelectric memory device, i.e. writing same state II to a first capacitor 76 and a second capacitor 78 (col. 6, lines 14-16 and col. 7, lines 1-11, Fig.5);
- baking the first capacitor 76 and the second capacitor 78 for a selected time (e.g. 20 hours) at a selected temperature (150 °C) (col. 6, lines 7-11);

- performing a same state (i.e. state I) read on the first capacitor 76 and the second capacitor 78 to obtain same state read data (col. 6, lines 11-13);
- comparing the same state read data with the written same state data by gathering the same state charge value, the writing and reading of an opposite complementary data state value (col. 6, lines 35-36);
- re-writing the same state read data (i.e. Qss) to the first capacitor 76 and the second capacitor 78 by repeating the writing step (col. 6, lines 37-39);
- waiting opposite state data (i.e. Qos) to the first capacitor 76 and the second capacitor 78;
- waiting a selected period of time so that the first capacitor 76 and the second capacitor 78 reach steady state, i.e. reaching a state that sufficiently receive a pulse sequence (col. 7, lines 14-28);
- performing an opposite state (i.e. Qos) read to obtain opposite state read data (col. 6, lines 23-26);
- comparing the opposite state read data with the opposite state data and to create a plot of these state read data as a function of time and temperature (col. 6, lines 35-39); and
- analyzing the obtained remaining charge data to determine data retention for the first state and the opposite state (col. 6, lines 30-39).

In re claim 13, Traynor also teaches that the same state (i.e. Qss) data is "0" for the first capacitor and "1" for the second capacitor and the opposite state (i.e. Qos) data is "1" for the first capacitor and "0" for the second capacitor (col. 2, lines 28-54).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2-5, 8, 9, 14 and 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Traynor in view of Kammerdiner et al. (US 5,969,935) and Mitra et al. (US 5,661,730).

In re claims 2-3, Traynor does not teach that the ferroelectric capacitor comprised of a bottom electrode, a top electrode, and a ferroelectric material in the respective memory cells, wherein the ferroelectric material is Pb(Zr,Ti)O3 (PZT).

However, Kammerdiner et al. teach that a well- known ferroelectric capacitor is comprised of a bottom electrode 36, a top electrode 40, and a ferroelectric material 38 in the respective memory cells, wherein the ferroelectric material 38 is PZT (col. 2, lines 18-24 and col. 1, lines 46-48).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to form the ferroelectric capacitor of Traynor having the top and bottom electrodes and the ferroelectric material, as taught by Kammerdiner et al., since top electrode/ferroelectric material/bottom electrode is a good configuration for ferroelectric capacitor to function properly.

In re claims 4-5 and 21-23, the selection of the data retention lifetime at different temperature is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species, as suggested by Mitra et al. (col. 7,

lines 41-43). In re Jones, 162 USPQ 224 (CCPA 1955)(the selection of optimum ranges within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980)(discovery of optimum value of result effective variable in a known process is obvious). In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range. See M.P.E.P. 2144.05, III

In re claim 9, Traynor does not teach performing a probe procedure that tests read/write capabilities of the memory cells.

However, Mitra et al. teach performing same state and opposite state in retention test and a probe procedure that tests read/write capabilities of the memory cells (col. 4, lines 33-49).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to perform the probe procedure, as taught by Mitra et al., in the method of Traynor, since by this manner it would provide a means for testing performance and reliability of the ferroelectric capacitor.

In re claim 14, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to recognize that retention test is a performance test before packaging the memory device, i.e. performing the retention test and further packaging the memory device. With this teaching, Traynor also teaches the limitations, as recited in claim 20, including selecting process time and temperature; performing data retention lifetime testing on the ferroelectric memory device; adjusting process time and temperature to improve data retention of the memory device; and packaging the memory device.

In re claims 8 and 19, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to recognize that Traynor also teaches that the initial state is selected to yield a data retention lifetime for the memory cells of the device that is greater than or equal to about the desired data retention lifetime because it is the purpose of the retention testing.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 571-272-1863. The examiner can normally be reached on M-F (9:00 ~ 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hsien-Ming Lee
Examiner
Art Unit 2823

March 6, 2004